

Fast and Accurate Transaction Level Models using Result Oriented Modeling

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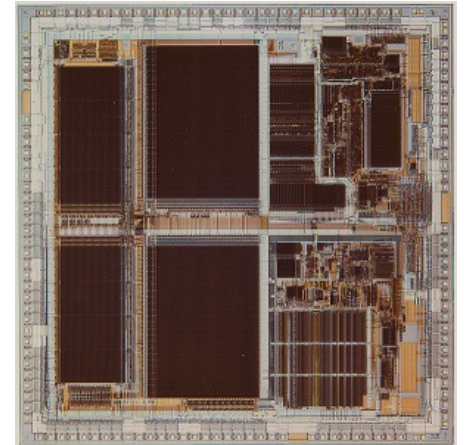
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Motivation

- Need high productivity in SoC design
 - Production capabilities increase
 - Time-to-market shortens
- Explore larger design space in less time
 - Requires fast simulation capabilities
- One approach: higher levels of abstraction
 - Transaction Level Modeling [T. Grötter et. al 2002]
 - Gains performance, but loses accuracy by abstraction
 - **TLM trade-off *speed vs. accuracy* [DATE 2006, IESS 2005]**
 - **either fast**
 - **or accurate**



Source: simh.trailing-edge.com

Goal

- **Eliminate the TLM trade-off**
 - 100% Accuracy
 - like a Bus Functional Model
 - Highest Speed
 - like TLM
- Based on a case study:
 - AMBA AHB 2.0



Outline

- Related Work
- Generic ROM Concept
- Modeling Example: AMBA AHB
 - Traditional Models
 - Novel ROM
 - Experimental Results
 - Accuracy
 - Performance
- Conclusions

Related Work

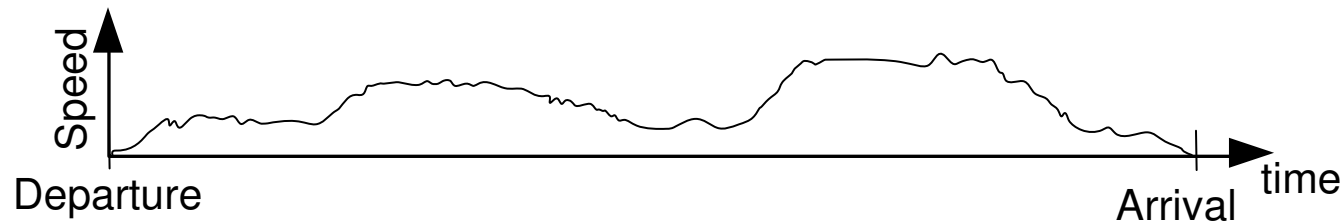
- Related Work
 - T. Grötter et al., *System Design with SystemC*. Kluwer Academic Publishers, 2002
 - M. Caldari et al., *Transaction-level models for AMBA bus architecture using SystemC 2.0*, DATE 2003
 - L. Cai and D. Gajski, *Transaction Level Modeling: An Overview*, CODES + ISSS 2003
 - M. Coppola et al., *IPSIM: SystemC 3.0 Enhancements for Communication Refinement*, DATE 2003
 - S. Pasricha et al., *Fast exploration of bus-based on-chip communication architectures*, CODES + ISSS 2004
 - ARM, *Amba AHB Cycle Level Interface specification*, ARM IHI 0011A
 - G. Schirner and R. Dömer, *Quantitative Analysis of Transaction Level Models for the AMBA Bus*, DATE 2006.

Generic ROM Concept

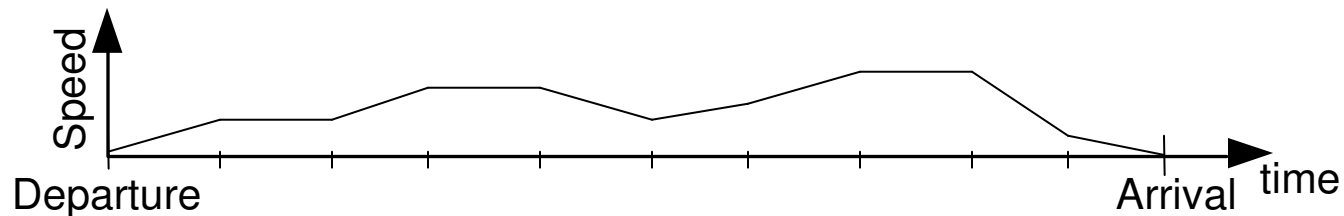
- Result Oriented Modeling (ROM)
- Illustrating Example:
Airplane Arrival Time



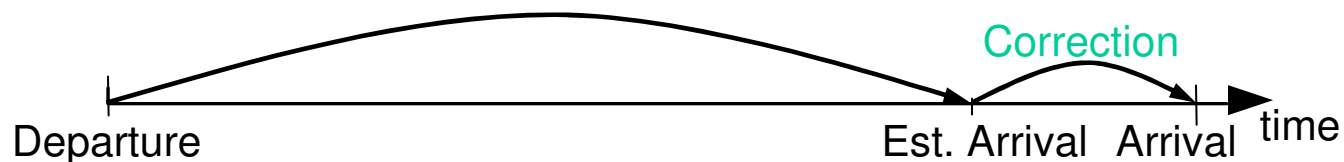
- **Reality:** Groundspeed changes with head wind



- **TLM:** Approximate in incremental steps

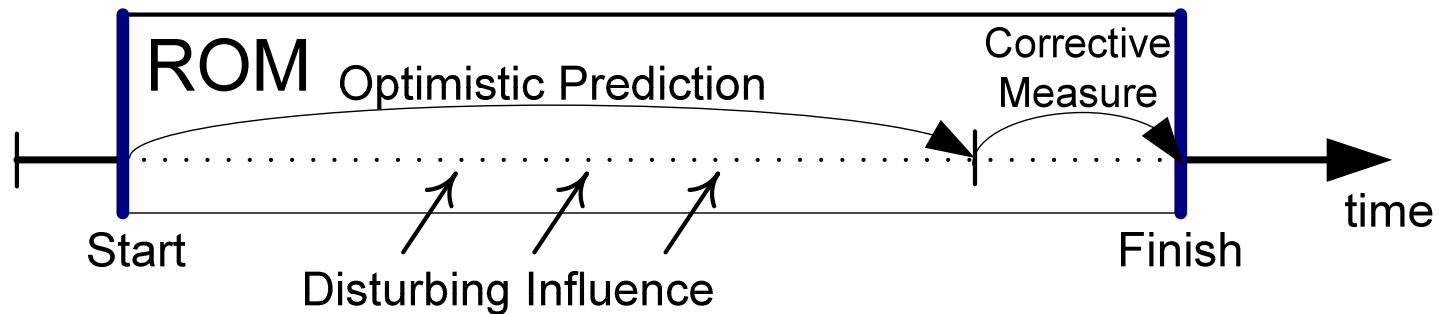


- **ROM:** Initial Prediction with correction at the end



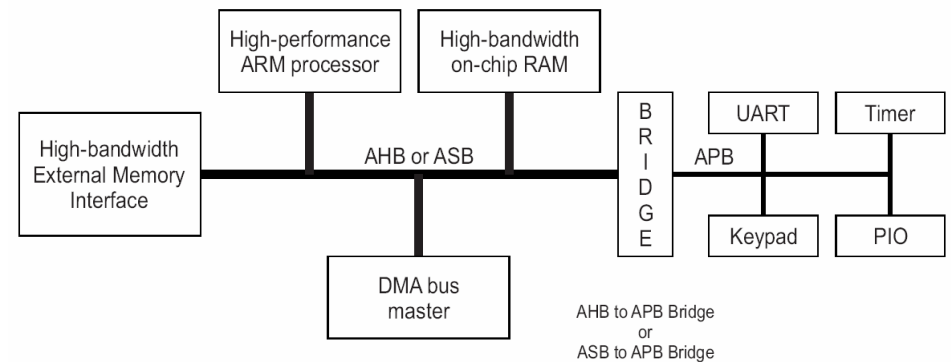
Generic ROM Concept

- Characteristics
 - Observability at boundary of transaction
 - Internal state changes not visible, may not modeled
 - *Optimistically predict* the *end result* at beginning
 - optimistic == earliest time to finish
 - Record *disturbing influence*
 - *Corrective measures* at the end



Modeling Example: AMBA AHB 2.0

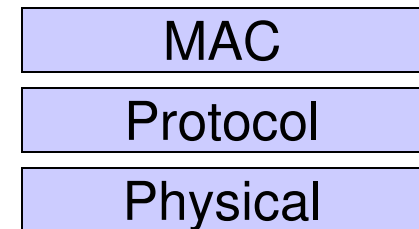
- **Advanced Microprocessor Bus Architecture (AMBA)**
 - De-facto standard for on-chip bus system
 - Hierarchical structure:
 - System bus + Peripheral bus
- **Advanced High-performance Bus (AHB)**
 - Multi-master bus
 - Pipelined operation
 - Burst transfers
 - Retry and split transactions
 - Multiplexed interconnection
 - Locked, unlocked transfers



Source: ARM

Traditional Models

- ISO/OSI reference layer-based architecture
 - see [DATE 2006]
 - Abstraction by:
 - Implementing fewer layers
 - Decreasing granularity
 - Larger blocks for arbitration + data handling
 - Three models:
 - TLM
 - ATLM
 - BFM



Traditional Models

1) Transaction Level Model (TLM)

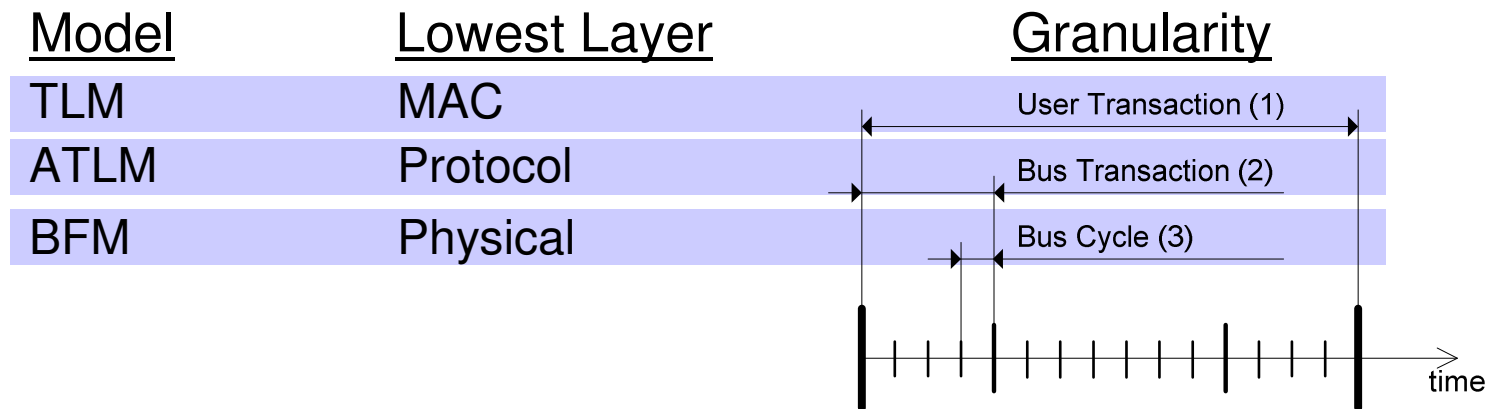
- User Transaction:
 - Contiguous block of bytes
 - Arbitrary length, base address

2) Arbitrated TLM (ATLM)

- Bus Transaction
 - Bus primitives (e.g. store word)
- Priority-based arbitration

3) Bus Functional Model (BFM)

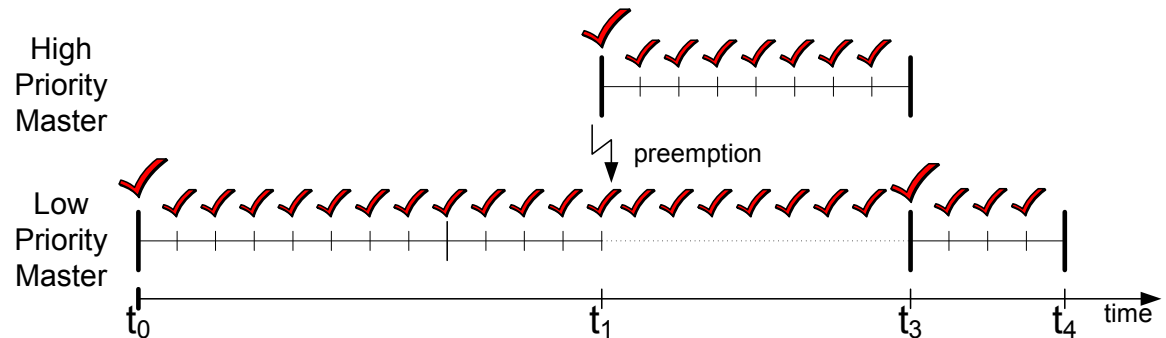
- Bus Cycle
 - Drive or sample bus wires on bus cycle



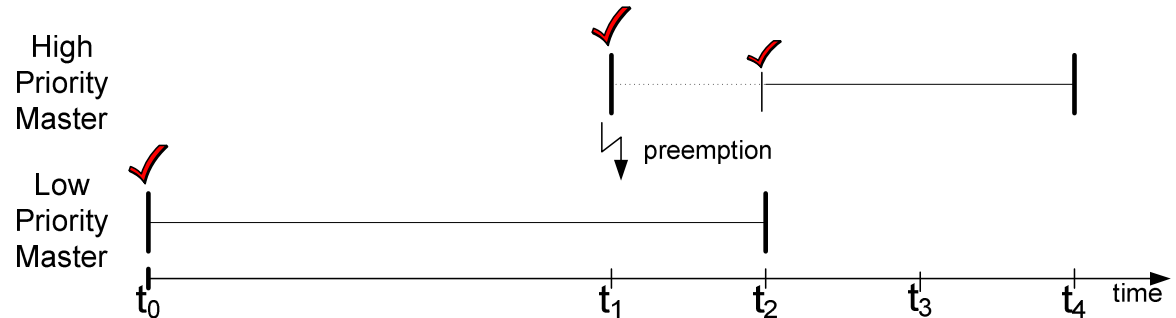
Traditional Models: Accuracy Limitations

- Example:
 - Low priority burst starting at t_0
 - High priority preemption at t_1

- BFM:
 - check every cycle
 - slow
 - accurate

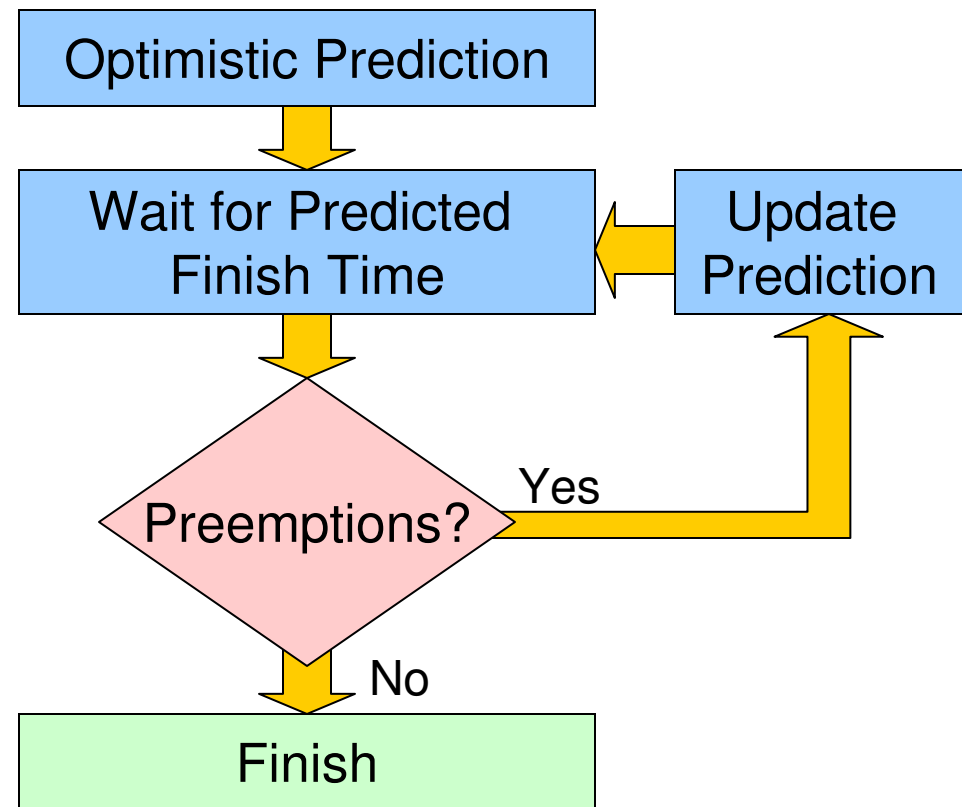
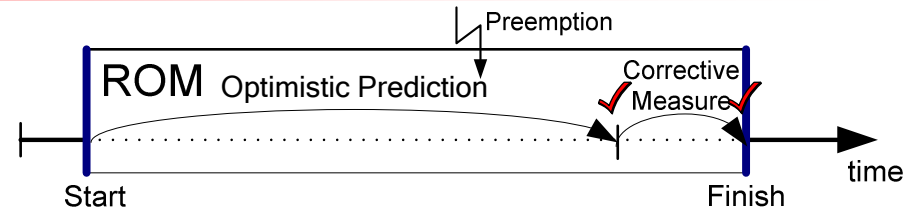


- TLM:
 - coarse grain check
 - fast
 - inaccurate:
low prio. burst
ends at
 t_2 instead of t_4



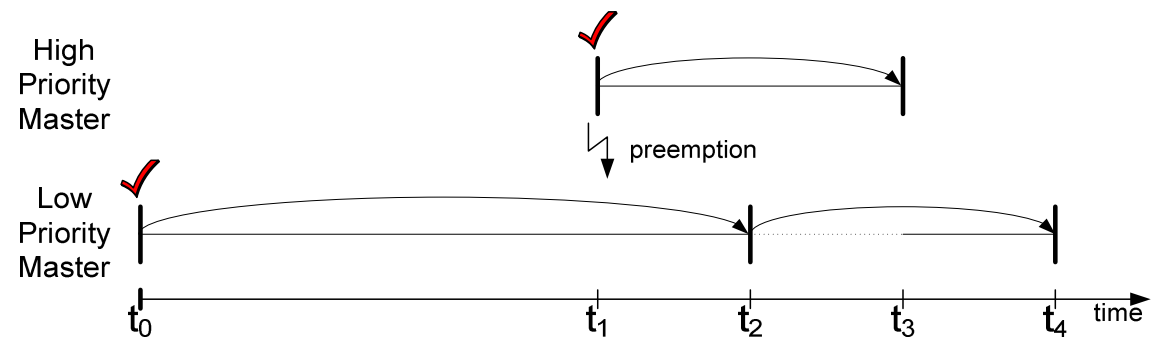
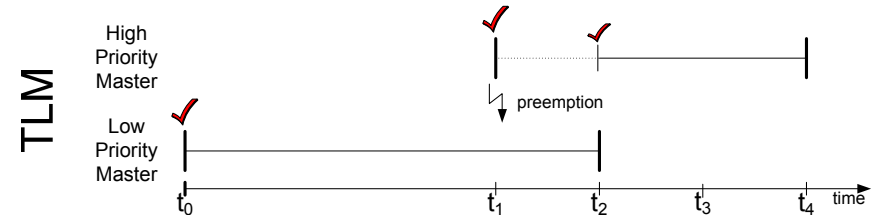
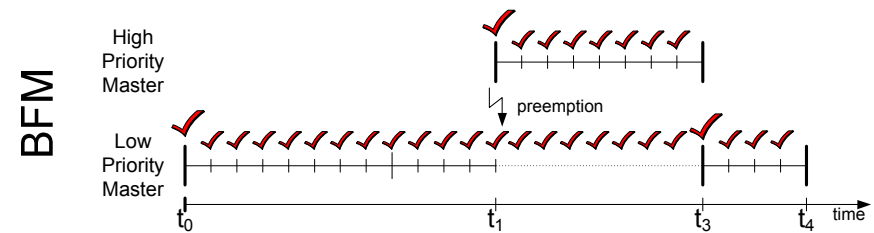
Result Oriented Modeling for AMBA AHB

- Assumption
 - Limited visibility
 - Functionality, Timing only at User Transaction boundary
- Omit or rearrange freely internal events
- **Optimistic Prediction**
 - Shortest possible duration
 - Start Time
 - Current bus state
 - Duration
 - Split into bus transactions
- **Wait for Predicted Finish Time**
 - Record preemptions
- **Check for Preemptions**
 - Update if required
- **Finish**
 - Copy data



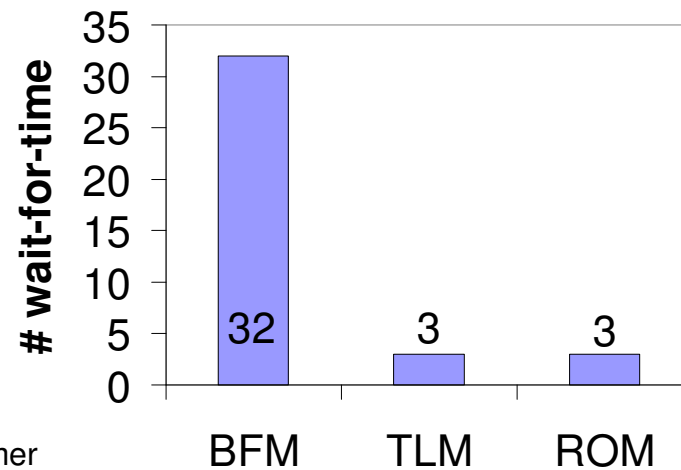
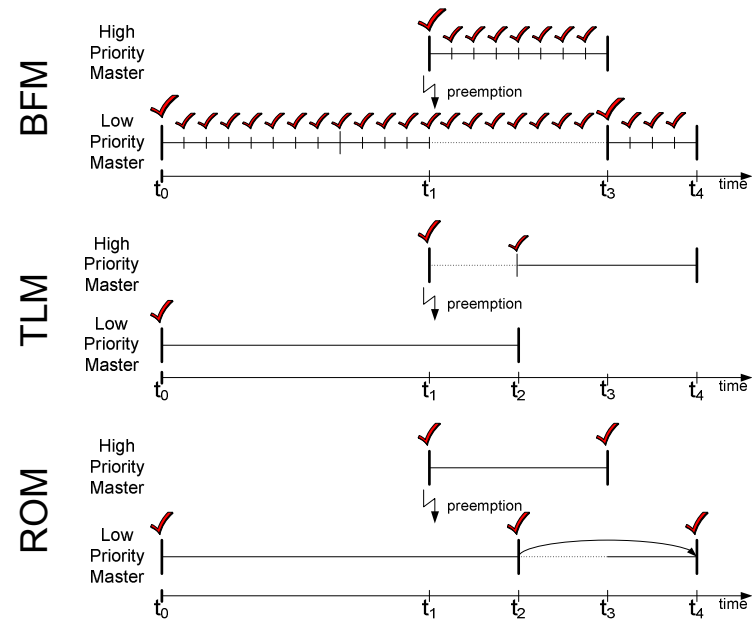
Result Oriented Modeling for AMBA AHB

- Same example transfer:
 - Low priority burst at t_0
 - High priority preemption at t_1
- ROM:
 - t_0 low: predict t_2
 - t_1 high: preempt, predict t_3 , record preemption for low
 - t_2 low: detect disturbance, prediction update t_4
 - t_3 high: no preemptions, finish
 - t_4 low: no preemptions, finish
 - **Accurate**



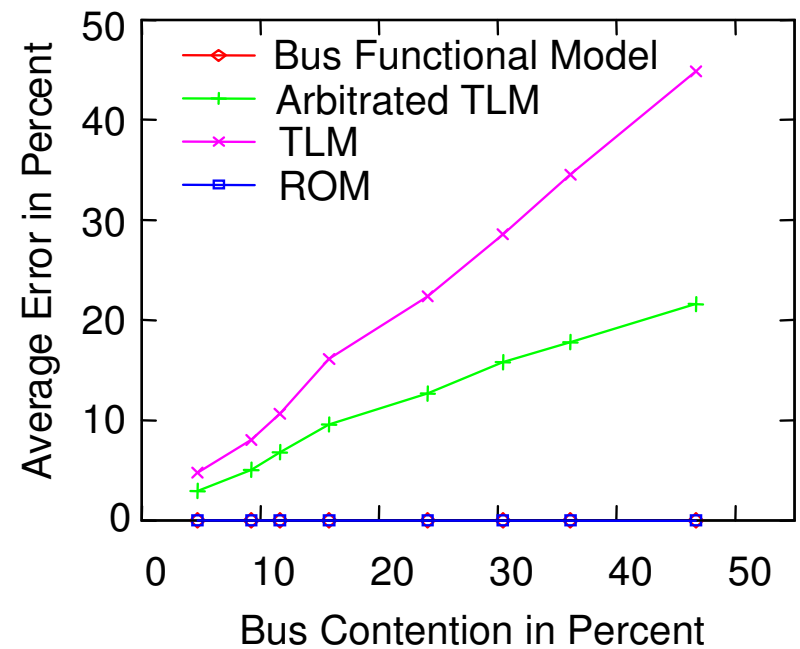
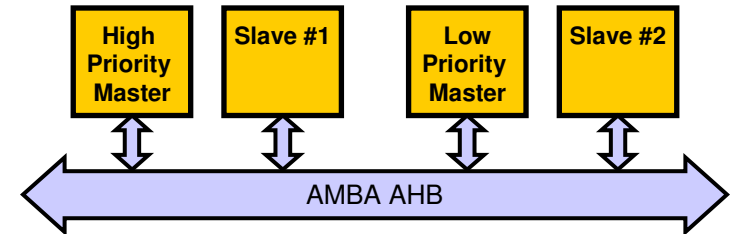
Result Oriented Modeling for AMBA AHB

- Performance expectation
 - Arbitration Check
 - requires a *wait-for-time* statement to advance simulated time
 - *wait-for-time*, often results in costly context switch
 - fewer *wait-for-time* → faster
 - Compare number of *wait-for-time*
 - Same example



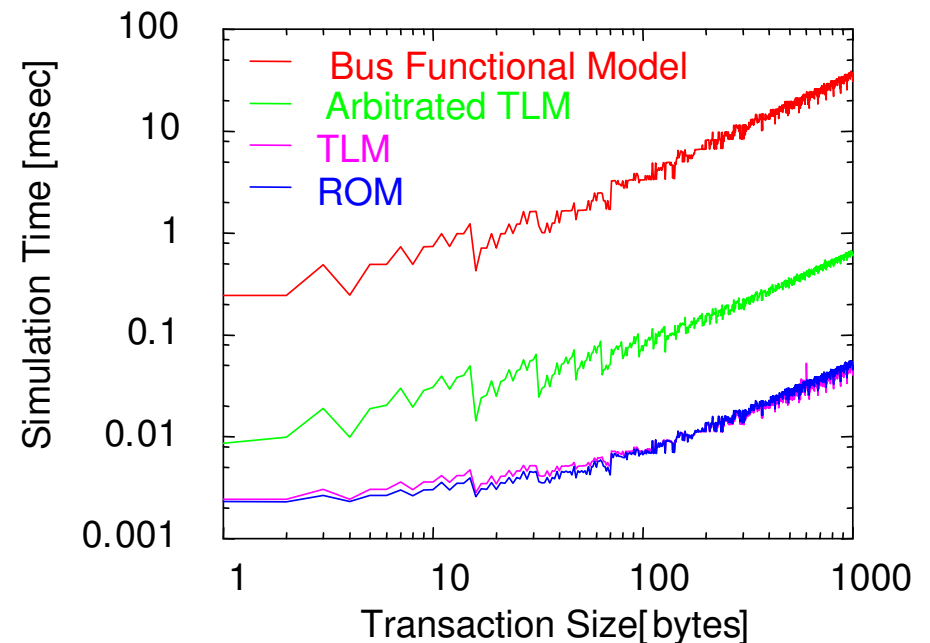
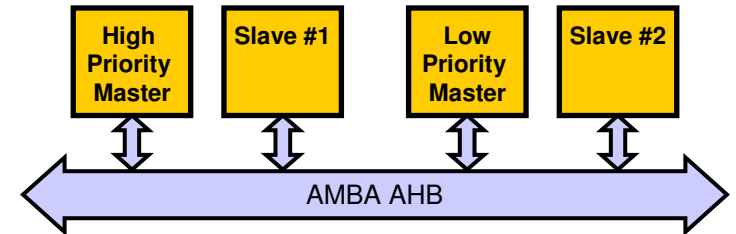
Experimental Results: Accuracy

- Average error in user transaction duration
 - 2 masters concurrently
 - Set of 5,000 user transactions each
 - Over increasing bus contention
 - Lower is better
- 100% Accuracy achieved!
 - ROM, BFM both on top of x-axis
 - No error
- Abstract models
 - Linear increasing error
 - TLM: up to 45%
 - ATLM: up to 22%



Experimental Results: Performance

- Simulation time
 - 2 concurrent masters
 - high priority: 33% bus load
 - measure low priority
 - Lower is better
- 100% Speed achieved!
 - ROM and TLM are equally fast!
 - 3 orders of magnitude faster than BFM



Conclusion

- Novel TLM Technique:
Result Oriented Modeling (ROM)
 - Observable only at transaction boundary
 - Optimistically predicts end result
 - Updates prediction at the end
- Applied to AMBA AHB 2.0
 - Experimental Results show the tremendous benefits
 - 100% accurate
 - 100% speed (i.e. speed like TLM)
- **ROM eliminates traditional TLM trade-off**
 - **Frees designer of model selection**
 - **Expands usability of TLM**