

# Defects and Fault Characterization in Quantum Cellular Automata

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## ABSTRACT

In this paper, a detailed simulation-based characterization of QCA defects and study of their effects at logic-level are presented. Different defect mechanisms for QCA active devices and interconnects are considered and the appropriate fault models at logic-level are investigated. Different implementations of QCA logic devices and interconnects are compared in term of defect tolerance and testability.

**Keywords:** Quantum Computing, Nano systems and devices, Defect Characterization

## 1 INTRODUCTION

There has been extensive research in recent years at nano scale to supersede CMOS technology. It is anticipated that these technologies can achieve a density of  $10^{12}$  devices/ $cm^2$  and operate at THZ frequencies.

Among these new devices, *quantum dot cellular automata* (QCA) not only gives a solution at nano scale, but also it offers a new method of computation and information transformation [5]. In terms of feature size, it is projected that a QCA cell of few nanometer size can be fabricated through molecular implementation by a self-assembly process. The unique feature of QCA based designs is that logic states are not stored in voltage levels as in conventional electronics, but they are represented by the position of individual electrons.

For QCA the cells must be aligned precisely at nano scales to provide correct functionality, so proper testing of these devices for manufacturing defects and misalignment plays a major role for quality of these circuits.

In this paper, the defect characterization of these devices has been extensively studied; the effects of defects at logic-level are investigated. Also, testing of QCA is compared with testing of conventional CMOS implementations of these logic devices.

The approach used in this work is based on simulating different manufacturing misalignments, investigating their effects at logic level and identifying the test vectors for fault detection. Different fabrication schemes of the majority voter at cell level are studied and compared in terms of defect tolerance and testability.

The rest of this paper is organized as follows. In Sec. 2, the defect characterization for QCA is presented.

In Sec. 3, test sets and defect and fault coverage are discussed. Finally, Sec. 4 concludes the paper.

## 2 DEFECT CHARACTERIZATION

In this section, the robustness of the QCA Majority Voters and Binary Wires is investigated. Various configurations of QCA devices are studied using the QCADesigner<sup>1</sup> v1.20 simulation tool. For accuracy, the bistable model is used, i.e. a quantum mechanical engine using Jacobi algorithm to calculate the eigenvalues/vectors of the Hamiltonian.

### 2.1 Defect and Failure Modes

To perform a defect characterization of QCA devices and circuits and study their effects at logic-level, appropriate defect mechanisms and models must be considered which 1) can be simulated using available simulation methods and 2) are realistic to model manufacturing and fabrication defects.

A *cell displacement* is a defect in which the defective cell is misplaced within its original direction. Several cell displacement defects are shown in Fig. 1. In a *cell misalignment* defect, the direction of the defective cell is misplaced. Some examples of cell misalignments are shown in Fig.2. In this paper, the following defects are simulated for QCA devices: all possible combinations of cell displacement with respect to the central cell under different distances, cell misalignment in different directions, and rotation.

### 2.2 Majority Voter Defect Analysis

The basic logic gate in QCA is the *majority voter* (MV). The MV with logic function  $MV(A, B, C) = AB + AC + BC$ , can be realized by only 5 QCA cells [5]. Logic AND and logic OR functions can be implemented from a majority voter by setting one input permanently to 0 and 1, respectively. In [5], [4] the design of a set of universal logic gates based on the majority voter and inverter gate is presented.

There has been a study of the fault tolerant properties of the MV under some manufacturing misalignments [1]–[3]. Based on this simulation-based study, a

<sup>1</sup>QCADesigner is the product of an ongoing collaboration between the ATIPS laboratory and University of Notre Dame.

fault tolerant MV block has been proposed. It has been shown that MV is more vulnerable to misalignment in the vertical direction than in the horizontal direction.

In this work, different defects in the MV (cell displacement and misalignment) are considered and simulated. The faulty results for cell displacement and misalignment are shown in Table 1 and 2, respectively. Only faulty entries are shown in the tables. The considered defect free majority gate has a  $5nm$  dot and a  $20nm \times 20nm$  cell size, with a  $5nm$  cell distance.

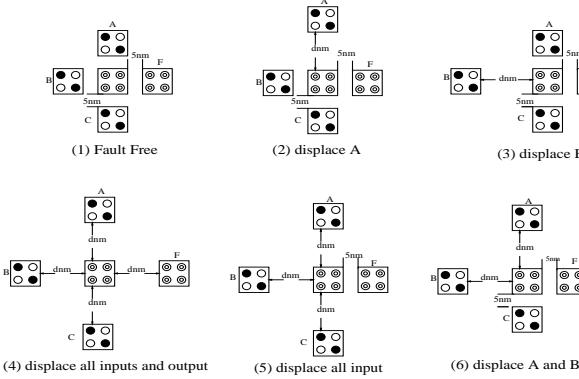


Figure 1: Displacement in Majority Voter

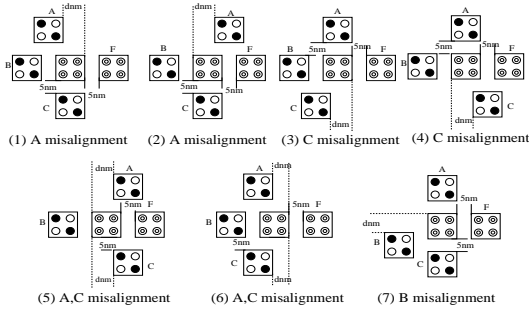


Figure 2: Misalignment in Majority Voter

The data shows that in most cases the horizontal input cell (i.e. cell B) is the dominant cell. For misalignment, any single cell misalignment greater or equal to half a cell causes malfunction (fault at logic-level). In some cases the error margin is even smaller.

### 2.3 Defect Analysis of Rotated Majority Voter

The simulation results show that MV is robust with respect to rotation of all input and output cells around the center cell, i.e. the logic-level behavior of the rotated MV is the same as the original device. Based on this observation, some simulations are performed to investigate the robustness of the rotated MV (RMV). The basic functionality of MVs is based on the Coulombic interaction among four neighboring QCA cells, which strongly depends on the precision and geometry of its implemen-

displace cell A: fig 1(2)		
$d \leq 15nm$ Normal Operation	$d \geq 20nm, F=B$	
displace cell B: fig 1(3)		
$d \leq 40nm$ Normal Operation	A B C	$d \geq 45nm$ F
	001	Z (no polarization)
	011	Z (no polarization)
	100	Z (no polarization)
	110	Z (no polarization)
displace all input/output cells: fig 1(4)		
$d \leq 10$ or $30 \leq d \leq 40nm$ Normal Operation	A B C	$15 \leq d \leq 25nm$ F
	010	0/1
$d \geq 45nm$ F=Z (no polarization)	101	1/0
displace all input cells: fig 1(5)		
$d \leq 15$ or $d = 40nm$ Normal Operation	$d \geq 45nm$ F=Z (no polarization)	
$20 \leq d \leq 25$ or $d = 35nm$	F	$d = 30nm$
A B C	F	A B C
010	0/1	000
101	1/0	010
		101
		111
		F
		0/1
		0/1
		1/0
		1/0
displace cells A and B: fig 1(6)		
$d \leq 5nm$ Normal Operation	$d \geq 10nm, F=C$	

Table 1: Results for displacement in Majority Voter

tation. We focus on validating different configurations of MV in the  $45^\circ$  rotation, as shown in Fig. 3.

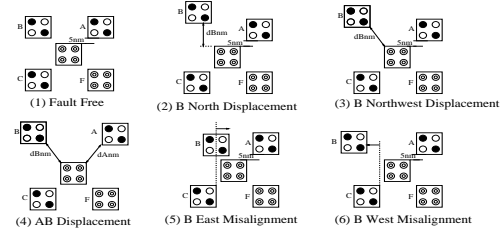


Figure 3: Rotated Majority Voter (Fault-free, with displacement or misalignment)

The simulation results show that the RMV functions normally, except when moving:

- A input north, with  $dA \geq 10nm$  for  $ABC = 001, 110$  (the output follows the C input). A similar output appears when moving A to northeast with  $dB \geq 10\sqrt{2}nm$ .
- B input north, with  $dB \geq 40nm$ . The output is unknown (unpolarized) for  $ABC = 001, 011, 100, 110$ . A similar output appears when moving B to the northwest with  $dB \geq 30\sqrt{2}nm$ .
- C input south, with  $dC \geq 15nm$  for  $ABC = 011, 100$  (the output follows the A input). A similar output appears when moving C to the southwest with  $dC \geq 10\sqrt{2}nm$ .
- A, B, C or A, B, C, Z away for  $d \geq 30\sqrt{2}nm$ . The output is undefined for all input combinations.
- A and B inputs away with  $d \geq 10\sqrt{2}nm$  for  $ABC = 001, 110$  (the output follows the C input).
- A and C inputs away with  $d \geq 10\sqrt{2}nm$  for  $ABC = 010, 101$  (the output follows the B input).
- B and C inputs away with  $d \geq 10\sqrt{2}nm$  for  $ABC = 011, 100$  (the output follows the A input).

move A toward west: fig 2(1)		
$d \leq 5nm$	Normal Operation	$d \geq 10nm, F=B$
move A toward east: fig 2(2)		
$5 \leq d \leq 15nm$	$d = 20$ or $d = 30nm$	Normal Operation $d = 25nm$ $F=A$
A B C	F	
001	0/1	
010	0/1	
101	1/0	
110	1/0	
move A,C toward west: fig 2(3)		
$d \leq 5nm$	$d \geq 10nm$	
Normal Operation $F=B$		
move C toward east: fig 2(4)		
$5 \leq d \leq 15nm$	$d = 20$ or $d = 30nm$	Normal Operation $d = 25nm$ $F=C$
A B C	F	
010	0/1	
011	1/0	
100	0/1	
101	1/0	
move A,C toward west: fig 2(5)		
$d \geq 5nm$	$F=B$	
move A,C toward east: fig 2(6)		
$d = 5, 20, d \geq 30nm$	$10nm \leq d \leq 15nm$	Normal Operation $F=B$
A B C	F	
000	0/1	
010	0/1	
101	1/0	
111	1/0	
move B toward south/north: fig 2(7)		
$d \leq 5nm$	$d \geq 45nm$	
Normal Operation		
A B C	F	
001	0/1	
011	1/0	
100	0/1	
110	1/0	

Table 2: Results for misalignment in Majority Voter

Cell misalignment defects for RMV are also considered (e.g., Fig. 3(5,6)). The following shows the results:

- Shifting the input A west (half/full cell size), leads the output F to follow input A, while shifting A east effects the output such that it follows input C.
- RMV functions normally when input B is shifted west for a half or full cell size. However, the output is undefined for inputs ABC = 001, 011, 100, 110 when  $dB \geq 40nm$ .
- The output follows the input B, when B is shifted east for a half or full cell size.
- The output follows the input A when C is shifted west, and follows C when C is shifted east.

### 2.3.1 OMV and RMV Comparison

The results for different configurations of the Original Majority Voter (OMV) and the Rotated Majority Voter (RMV) are illustrated in Table 3. MV is completely robust with respect to rotation of all inputs and output cells around the central cell. This gives a significant degree of freedom for synthesizing designs based on QCA, as RMV can be used as the Original Majority Voter block. However, the original block is more dependent on the middle input (B) than the other inputs (A and C), in terms of displacement and misalignment. In the rotated version, this dependency can be completely changed based on the degree of rotation. An overall comparison in the table confirms that RMV is more fault-tolerant than the Original MV. Note that

only half and full misalignments are considered.

Config.	Faults	OMV	RMV
A move	distance	$d \geq 20nm$	$d \geq 10(N)$ or $10\sqrt{2}nm$ (NE)
	# of faults	2	2
B move	distance	$d \geq 45nm$	$d \geq 40(W)$ or $30\sqrt{2}nm$ (NW)
	# of faults	4	4
C move	distance	$d \geq 20nm$	$d \geq 10(S)$ or $10\sqrt{2}nm$ (SW)
	# of faults	2	2
ABC move	distance	$20 \leq d \leq 35$ or $d \geq 45nm$	$d \geq 30\sqrt{2}nm$
	# of faults	2/4/8	8
ABCF move	distance	$15 \leq d \leq 25$ or $d \geq 45nm$	$d \geq 30\sqrt{2}nm$
	# of faults	2/8	8
AB move	distance	$d \geq 7.5nm$	$d \geq 10\sqrt{2}nm$
	# of faults	2	2
AC move	distance	$d \geq 7.5nm$	$d \geq 10\sqrt{2}nm$
	# of faults	2	2
Z move	distance	$d \geq 45nm$	$d \geq 30\sqrt{2}nm$
	# of faults	8	8
AC misalignment	# of faults	4	4
B misalign. West	# of faults	4	0
B misalign. East	# of faults	4	2

Table 3: Original Majority Voter vs. Rotated Majority Voter

## 2.4 Binary Wires and Inverter Chains

The effect of cell displacement defects on two parallel binary wires as well as two parallel inverter chains are investigated.

### 2.4.1 Double Binary Wires

Two defect-free binary wires are shown in Fig. 4(a); the wires are denoted as the upper wire ( $i1$  to  $o1$ ) and the lower wire ( $i2$  to  $o2$ ). The cells have a size of  $20nm \times 20nm$ , and the dot diameter is  $5nm$ . In the defect-free case, the cells in the same wire are separated by  $15nm$  and the wire distance is  $60nm$ .

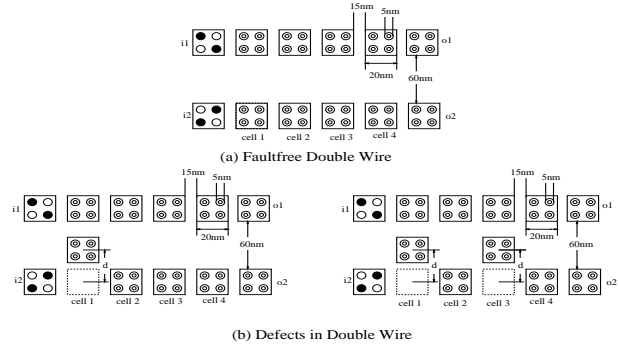


Figure 4: Displacement in Binary Double Wires

The displacement defects are simulated by moving one or two cells in the lower wire toward the upper wire (by displacement  $d$ ) as shown in Fig. 4(b).

The simulation results are shown in Table 4. The results show that the upper wire is dominant in most cases:  $o1$  and  $o2$  are either equal to  $i1$  or  $i1'$ , depending on which cell(s) are displaced and the value of the displacement,  $d$ . In most cases, the upper wire functions normally, i.e.  $i1 = o1$ . However, in some cases the upper wire behaves as an inverter. Clearly, unlike CMOS

designs, the coupling defects at QCA device-level do not behave as the *wired bridging fault* model. However, these defects manifest themselves as the dominant model (at logic level) in which the output of a wire is determined by the value of the coupled wire.

move cell1 OR cell2				
$d \leq 40nm$	$d = 45 - 50nm$	$d \geq 55nm$		
Normal	$o1 = i1, o2 = i1$	$o1 = i1, o2 = Z$		
move cell3 OR cell4				
$d \leq 35nm$	$d = 40 - 50nm$	$d \geq 55nm$		
Normal	$o1 = i1, o2 = i1'$	$o1 = i1, o2 = Z$		
move cell1 AND cell2				
$d \leq 35nm$	$d = 40 - 50nm$	$d \geq 55nm$		
Normal	$o1 = i1, o2 = i1$	$o1 = i1, o2 = Z$		
move cell1 AND cell4; OR move cell 2 AND cell 3; OR move cell3 AND cell4				
$d \leq 35nm$	$d = 40 - 50nm$	$d \geq 55nm$		
Normal	$o1 = i1, o2 = i1'$	$o1 = i1, o2 = Z$		
move cell1 AND cell3				
$d \leq 35nm$	$d = 40 - 50nm$	$d = 45nm$	$d \geq 55nm$	
Normal	$o1 = i1, o2 = i1$	$o1 = i1, o2 = i1'$	$o1 = i1, o2 = Z$	
move cell2 AND cell4				
$d \leq 15nm$	$d=20-25nm$ $d=40-45nm$	$d=30-35nm$	$d = 50nm$	$d \geq 55nm$
Normal	$o1 = i1$	$o1 = i1$ $o2 = i1$	$o1 = i1'$ $o2 = i1$	$o1 = i1$ $o2 = Z$

Table 4: Results for Double Binary Wires

### 2.4.2 Double Inverter Chains

The double inverter chain is shown in Figure 5(a). The simulation results for moving one cell in the bottom wire toward the upper wire, with displacement  $d$ , (Figure 5(b)) are presented in Table 5. The displacement defects behave as the *dominating bridging fault* model at logic level. Moreover, a comparison with the binary wires shows that binary wires are more defect tolerant than inverter chains in case of displacement coupling defects.

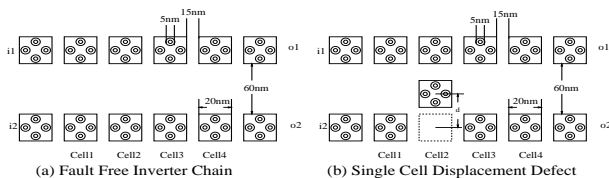


Figure 5: Displacement in Double Inverter Chains

Fault Free: $o1 = i1'; o2 = i2'$		
move cell1 OR cell2 OR cell3		
$d \leq 35nm$	$d = 40nm - 50nm$	$d \geq 55nm$
Normal	$o1 = i1', o2 = i1'$	$o1 = i1', o2 = Z$
move cell4		
$d \leq 30nm$	$d = 35nm - 50nm$	$d \geq 55nm$
Normal	$o1 = i1', o2 = i1'$	$o1 = i1', o2 = Z$

Table 5: Results for Double Inverter Chains

## 3 TEST SETS, DEFECT COVERAGE AND FAULT MODEL

The effectiveness of different stuck-at test sets is evaluated for the simulated defects on a single majority voter. The main results are as follow:

- In all simulations, *super exhaustive* input patterns (i.e. all possible input transitions) are used. The

results show that there is no sequence dependent behavior at logic level; i.e. none of the manufacturing misalignments introduces a state dependency.

- Except for a single case (i.e. the displacement of all inputs and output cells) faults are detected using a subset of some 100% stuck-at fault test sets. Note that not all of these 100% stuck-at test sets are the same.
- A particular 100% 2-detect stuck-at test set (each fault is detected by two vectors) can detect all manufacturing defects, except for the simultaneous displacement of the top and left inputs.
- Moreover, a particular 100% single stuck-at test set (001,010,011,101) can detect all simulated defects.

## 4 CONCLUSIONS

Quantum dots cellular automata (QCA) are novel devices which are promising in the era of nano scale computing. In this paper, a detailed defect characterization for QCA logic devices and some representative circuits has been presented. As shown in this paper, the coupling mechanisms and behavior of defects at logic-level (i.e. the faults) are not similar to those for conventional CMOS. The effectiveness of different stuck-at test sets in detecting QCA defects has been studied. Our results show that to achieve a high defect coverage, the specific QCA implementation of each function must be considered for test generation.

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