

## Frequency Domain Measurement of Timing Jitter in ATE

L. Schiano<sup>1</sup>, M. Momenzadeh<sup>1</sup>, F. Zhang<sup>1</sup>, Y. J. Lee<sup>1</sup>, Y-B. Kim<sup>1</sup>, F. Lombardi<sup>1</sup>, F. J. Meyer<sup>2</sup>, T. Kane<sup>3</sup>,  
S. Max<sup>3</sup>, P. Perkins<sup>3</sup>

<sup>1</sup> ECE Department,  
Northeastern University,  
Boston MA 02115, USA

E-mail: {lschiano, mmomenza, fzhang, yjlee, ybk, lombardi}@ecc.neu.edu

<sup>2</sup>Wichita State University,  
Wichita KS 67260, USA  
Email: fred.meyer@wichita.edu

<sup>3</sup>LTX Corporation,  
Westwood MA 02090  
Email: {thomas.kane, sol.max, phil.perkins}@ltx.com

**Abstract** – The objective of this paper is to provide a framework by which jitter phenomena, which are encountered at the output signals of a head board in an automatic test equipment (ATE), can be studied. In this paper, the jitter refers to the one caused by radiated electromagnetic interference (EMI) noise, which is present in the head of an ATE due to DC-DC converter activity. An initial analysis of the areas of the head board most sensitive to EMI noise has been made. It identifies a sensitive part in the loop filter of a phase locked loop which is used to obtain a high frequency clock for the timing generator. Different H-fields are then applied externally at the loop filter to verify the behavior of the output signal of the head board in terms of RMS jitter. As for RMS jitter measurements, a frequency domain methodology has been employed. A trend for RMS jitter variation with respect to radiated EMI magnitude as well as frequency has been obtained. Also the orientation of the external H-field source with respect to the target board and its effects on the measured RMS jitter has been investigated. For measuring the RMS value, a proper circuitry has been designed on a daughter board to circumvent ground noise and connectivity problems arising from the head environment.

**Keywords** – Automatic Test Equipment, jitter measurement, jitter characterization in frequency domain, test head board, EMI induced jitter.

### I. INTRODUCTION

To meet the challenges of designing and testing modern integrated circuits, Automatic Test Equipment (ATE) architectures have undergone radical changes in operation and design [2]. While past ATE architectures were based on shared resources (i.e., all channels shared test processor, pattern generator and timing generator (TG)), in the last decades so-called Per-pin architectures have been developed to provide more flexibility by allocating to each channel its own TG. In this

architecture, all components except the test processor are integrated on a single board. Recently, ATE architectures have been designed based on a Per-pin Test Processor architecture, in which nearly all system components are integrated onto a single chip.

This evolution has provided excellent test flexibility and compactness, and has lowered the per-chip test cost. However, the new generation of ATEs requires high frequency operation for testing high performance device-under-test (DUTs) with no compromises in timing uncertainty. Therefore, the output signal integrity in these ATE systems has become a critical issue, because the clock speed of the IC's under test is in the Giga Hertz region. As ATEs provide the necessary instrumentation for the generation of tests and signals to device-under-test (DUT) with high operating frequency, jitter has become a critical parameter [3]. In multi-site testing, the quality and repeatability of the timing requires very low jitter to get reproducible test results. In order to guarantee the quality of the system, an evaluation of the timing jitter must be performed. If the jitter is excessive, steps must be taken to reduce it.

Among signal integrity problems, jitter variation due to radiated electromagnetic interference (EMI) from switching power supplies has come to prominence and is addressed in this paper. The goal of this paper is to provide, by means of an experimental modeling, the framework by which jitter variation due to radiated EMI can be predicted. A measurement methodology as well as a qualitative analysis (based on experimental results) are proposed. In particular, while in [1] was proposed a time domain based technique to measure the timing jitter, in this work frequency domain based measurements have been employed.

The remaining sections are organized as follows: Section 2

discusses the basic issues associated with the signal integrity problem revolving around DC-DC converters. Furthermore, it introduces an analytical model for jitter which is amenable to a frequency domain measurement approach. A methodology for measuring the jitter due to radiated EMI is then proposed in Section 3, followed by experimental results in Section 4. Finally, conclusions are drawn in Section 5.

## II. SIGNAL INTEGRITY PROBLEM AND JITTER CHARACTERIZATION

This section introduces jitter problems due to radiated EMI noise in the head board of an ATE and outlines a model for the proposed analysis.

### A. Head Board and Signal Integrity Problem

An ATE consists of a power supply module, the chiller system, a reference clock generator, and multiple head boards such as the shown in Fig. 1.

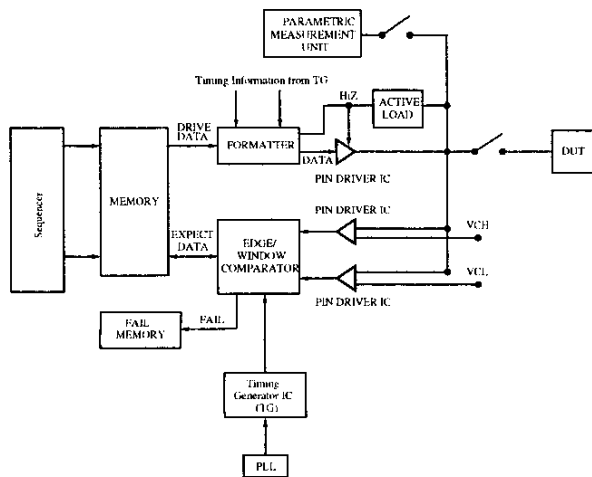


Fig. 1. Block diagram of a head board in an ATE

The test head board consists of memories, test pattern generator, timing generator, pin electronics, and programmable parametric measurement function units. The memories store the test vectors and the measured data collected from the DUT. The pattern and timing generators provide patterns and timing signals, respectively. The pin electronics circuitry merges the timing, pattern and format information to drive the DUT pin and compare the DUT outputs with the expected data. The programmable parametric measurement unit acquires the DC output parameters from the DUT.

As the head board is made of various components (whose supply voltage levels are likely to be different), DC-DC converters are also required. The use of DC-DC converter has several advantages: i) its size is small and it can be mounted on a printed circuit board (PCB); ii) it can generate virtually any desired voltage level, independently of the input level; iii)

it is usually cheaper and much more efficient than linear power supply modules.

However, converters may cause EMI in the head board due to its switching characteristics [4] and, therefore, the jitter of the test signal may be increased. At today's operating frequencies, the timing margin of the test measurement has significantly decreased. In general, the timing margin will become worse due to the increasing clock speed by which the ATE must operate for testing the DUT. Eventually, this can have a catastrophic impact on the test outcome as a good DUT could be diagnosed as faulty due to jitter invalidating the timing measurement.

### B. Phase Noise Model

Jitter is usually defined as the *deviation* in the transition of the signal from its desired (ideal) position. An extensive treatment of jitter can be found in [6] [7].

In this work, the Phase Noise Model has been adopted to characterize the jitter [7]. For limited jitter phenomena, as in the considered case, the model allows to estimate the time domain property from noise spectrum measurements using a spectrum analyzer. This method is very convenient for high frequency signals.

The Phase Noise Model is illustrated for a sinusoidal clock. By analyzing only the fundamental component of a square-wave signal (as target signal) a good jitter analysis can be obtained [7].

In the Phase Noise Model, the jittering signal is modeled by the phase modulated signal as

$$x(t) = A_c \cos[\omega_c t + \theta(t)] \quad (1)$$

where  $A_c$  and  $\omega_c$  are the amplitude and angular frequency of the carrier (i.e. the fundamental component of the target signal) respectively. From Eq.1 the phase noise can be expressed as timing jitter by

$$\Delta t_{jitter} = \frac{\theta(t)}{\omega_c} \quad (2)$$

Furthermore, for small phase noise, Eq.1 can be formulated as:

$$x(t) = A_c \cos \omega_c t - \theta(t) A_c \sin(\omega_c t) = v_s(t) + v_n(t). \quad (3)$$

where  $v_s(t)$  and  $v_n(t)$  are the signal and noise components of the jittering signal respectively. Eq.3 shows, in a frequency domain, the jitter as baseband noise spectrum which is translated by an ideal signal frequency.

From the previous equation it follows that:

$$\langle v_n(t)^2 \rangle = \frac{A_c^2}{2} \langle \theta^2(t) \rangle. \quad (4)$$

By considering Eq.2 and Eq.4, then

$$TimingJitter_{RMS} = \frac{\theta_{RMS}}{\omega_c} = \frac{v_{nRMS}}{2\pi f A_c}. \quad (5)$$

Eq.5 translates the jitter spectral components (measured through a spectrum analyzer) to a time domain.

### III. EXPERIMENTAL SETUP AND METHODOLOGY

In this section, a methodology for measuring the jitter is proposed. To account for the compact nature and placement of the boards in the head of an ATE, a daughter board has been designed for measuring the jitter.

#### A. Experimental Procedure

To measure the jitter as affected by the radiated EMI on the head board, the following procedure is proposed.

1. **H-field emissions measurement from the board:** The H-field is measured on a fully powered head board near the DC-DC converters, with a close-field probe and a spectrum analyzer [8]. In addition, H-field emissions are measured at other locations on the board.
2. **H-field generation:** Using a coil and a function generator, the H-field is forced along the test signal generation path which consists of the PLL, the clock distribution IC's, the timing generator IC, and the time vernier IC.
3. **Jitter measurement:** The jitter is measured while applying the various H-fields to the signal generation path. To ensure that the measured jitter is only due to the forced H-field, the latter is generated for frequencies at which no other spectral component was previously identified.
4. **Analysis:** The ratio of the applied H-field to the originally measured H-field is an indication of the sensitivity of the timing in the presence of the DC-DC converters. A trend for the measured jitter with respect to EMI noise magnitude and frequency is then drawn and some qualitative results about jitter dependency with respect to the H-field generator orientation and the target board are presented.

#### B. Daughter Board Design

To accurately measure the jitter of a signal, it is necessary to carefully check the fixture of the signal interconnections and to consider issues such as connectivity, ground noise and impedance matching.

Thus, to have trustworthy experimental results, connections must be stable, ground noise must be avoided and impedance matching in the transmission path must not be impaired. An auxiliary daughter board (as presented in [1]) has been used to overcome these problems. This board is compatible with the head board and allows ATE operation. A circuit diagram of the daughter board is shown in Fig.2.

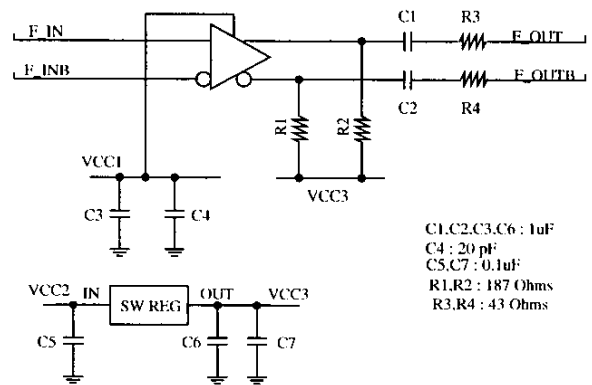


Fig. 2. Circuit diagram of the auxiliary daughter board

This circuit consists of a buffer circuit, a switching power supply module, several capacitors (power and coupling), and termination resistors.

The input signal frequency  $F_{IN}$  (Fig.2) is greater than 1GHz and the power supply comes from the test head board. The various components are described as follows:

- $C_{1,2}$  are AC coupling capacitors;  $C_{3,4}$ ,  $C_{5,6}$  and  $C_7$  are used as power bypass capacitors for the various power supplies.
- Some supply voltages come from the test head board; The supply power for the buffer circuit is generated from the small switching power supply module on the board.
- $R_{1,2}$  are pull-down resistors, and their values are 187  $\Omega$ .  $R_{3,4}$  are back-matching resistors whose values are 43  $\Omega$ ; together with the internal 7  $\Omega$  resistance of the buffer, this accomplishes the 50  $\Omega$  impedance matching.
- As the board thickness is 0.063", the trace width to make a 50  $\Omega$  impedance is 0.110" [9].
- A MMCX connector is used, because the space between the daughter board and the head board is very tight.

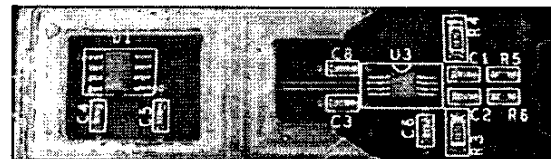


Fig. 3. Photograph of the daughter board

A picture of the daughter board is shown in Fig. 3.

### IV. EXPERIMENTAL MEASUREMENTS AND RESULTS

Experimental measurements and results obtained with the proposed procedure are now presented in more detail.

#### A. On-board DC-DC Converter Emission Measurements

To measure the emissions from the DC-DC converters, the following equipment is used: a commercial close field probe, a pre-amplifier and a spectrum analyzer.

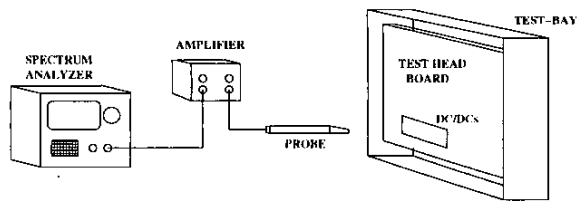


Fig. 4. Experimental set-up to measure the DC-DC converter emission

TABLE I  
MEASURED H-FIELD FROM THE DC-DC CONVERTERS

Frequency[KHz]	H-Field[dB $\frac{\mu A}{m}$ ]
198	131.1
198	120.86
204	130.27

The measurement method employed for the head board is similar to the one described in [8]. Fig. 4 shows the experimental setup. The close-field magnetic probe, applied close to the DC-DC converters, reveals the radiated H-field. The probe's output is connected to a pre-amplifier and then to the spectrum analyzer. The gain of the signal paths (including pre-amplification and the probe antenna factor) are considered for accurate H-field measurements.

All frequencies up to 1 GHz have been scanned to find the spectral components of the produced emissions. The measured results show that the peak of the H-field occurs at around 200 KHz, which is the same as the switching frequency of the three DC-DC converters used in the board. The experimental results are given in Table I. Very little energy was observed at frequencies above 1MHz.

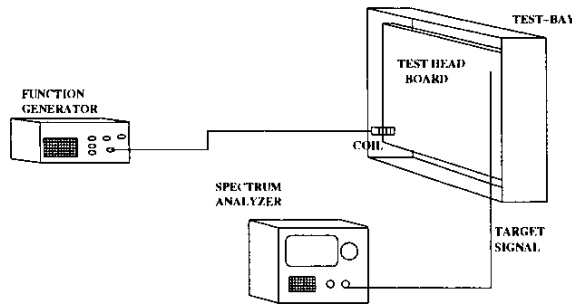


Fig. 5. Jitter measurement configuration

### B. Jitter Measurement: Experiment Description

The experimental configuration for the measurement of the jitter is shown in Fig. 5.

After the experimental configuration is set up, an external H-field is forced to reveal the most sensitive part in the board. As for the external H-field generator, a coil has been made by turning a thin wire in a three layer structure. The coil is also

TABLE II  
H-FIELDS [A/M] AT DIFFERENT FREQUENCIES GENERATED BY GIVING AT THE COIL INPUT A SINUSOIDAL SIGNAL LINEARLY INCREASING FROM  $1V_{pp}$  TO  $10V_{pp}$ , WITH A  $1V_{pp}$  STEP.

$V_{pp}$	250 KHz	500 KHz	1 MHz
10	1579.43	782.53	360.16
9	1425.61	707.13	325.09
8	1273.5	630.96	289.40
7	1115.58	553.35	254.68
6	959.40	476.43	218.78
5	803.53	398.57	183.02
4	646.40	320.26	147.06
3	484.17	240.16	110.28
2	320.63	159.40	73.20
1	161.25	79.89	36.81

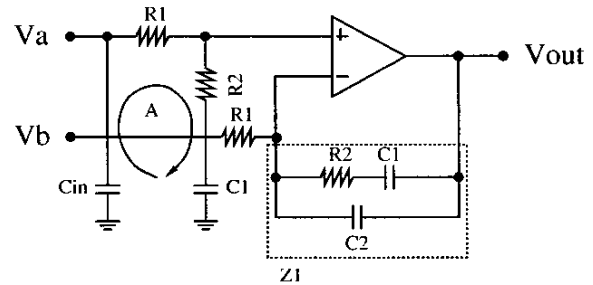


Fig. 6. Loop filter of the phase locked loop

shielded with respect to the E-field, to prevent capacitive coupling effects with the board. Therefore, only the H-field contribution to the measured jitter has been considered. As mentioned before, we generate H-fields of different frequency and magnitude. Table II shows the obtained values with sinusoidal input signals at 250 KHz, 500 KHz and 1 MHz respectively, and amplitude linearly increasing from  $1V_{pp}$  to  $10V_{pp}$ . According to Table II, due to the coil characteristic impedance, higher values of H-field and wider ranges are generated at smaller frequencies. However, at each frequency the induced jitter can be obtained with respect to EMI magnitudes.

Hereafter, unless specified, the external H-field is intended to be generated by the coil with its magnetic axis perpendicular to the board plane. However, a qualitative analysis of the effects by considering different orientations is also discussed.

The most sensitive part is identified in the loop filter of the timing generator's PLL, shown in Fig. 6. In particular, a high sensitivity to EMI occurs when the external H-field generator is applied close to the closed loop A, made by R1, R2, C1 and  $C_{in}$  in Fig. 6.

Fig. 7 shows the two spectra around the fundamental component of the target signal before and after applying a 250 KHz external H-field to the PLL loop filter. When the external H-field is applied, a component appears at a distance of 250 KHz from the fundamental, as expected from the Phase Noise Model for the jitter (Eq.3, Sec.2.2). Spuria visible in the spec-

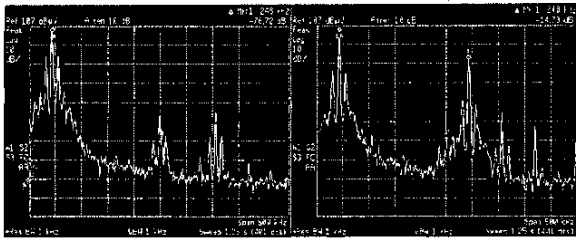


Fig. 7. Spectra around the fundamental component of the target signal before and after the application of the external H-field.

TABLE III

THE MEASURED RMS JITTER BY APPLYING H-FIELDS OF DIFFERENT MAGNITUDE AT DIFFERENT FREQUENCY

250 KHz		500 KHz		1 MHz	
Magn. [A/m]	Jitter [ps]	Magn. [A/m]	Jitter [ps]	Magn. [A/m]	Jitter [ps]
2789.33	39.55	1638.7	19.46	811.90	8.95
2532.21	35.74	1527.57	17.52	755.96	8.12
2272.48	31.92	1378.80	15.65	687.07	7.13
1997.56	27.97	1220.39	13.71	608.84	6.29
1719.89	23.86	1051.96	11.64	526.62	5.35
1437.14	19.91	883.08	9.75	445.14	4.45
1154.78	15.78	709.58	7.8	356.86	3.58
867.96	11.74	533.33	5.81	268.23	2.67
579.43	7.81	356.45	3.89	179.89	1.78
288.74	3.94	178.65	1.96	89.33	0.90

trum not corresponding to any application of external noise are due to EMI effects from the on-board circuitry. To clearly identify the applied H-field (as cause of a measured spectral component) frequencies at which no spectral component is found with no H-field injection must be analyzed. The chosen frequencies are consistent with trends of head board design.

### C. Jitter Measurements: Results

Starting from the values observed for the DC-DC converter emission, H-fields of increasing magnitude are generated at different frequency. This noise is applied to the head board to investigate its effects on the RMS jitter of the board output signal.

While applying H-fields with magnitude similar to the measured DC-DC emission, the observed jitter is tolerable. Significant RMS jitter values are obtained with H-fields of higher magnitudes, as describing worst case scenario in the ATE.

The applied H-fields and the corresponding measured RMS jitter values are shown in Table III and Fig.8. This shows a linear dependency of the measured jitter with the H-field magnitude. Moreover, the slope of the curves decreases when the frequency increases, thus showing a higher sensitivity of the jitter phenomena to lower EMI noise frequencies. This behavior is valid for frequencies up to 1MHz. For higher frequencies of EMI noise (not considered in this paper) the amount of jitter increased.

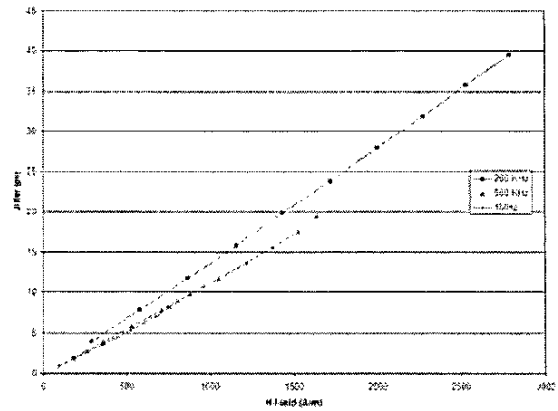


Fig. 8. Measured RMS jitter by applying H-fields of different magnitude at different frequency

TABLE IV

THE MEASURED RMS JITTER APPLYING A  $173dB\mu A/m$  H-FIELD AT DIFFERENT FREQUENCIES

Frequency [KHz]	RMS Jitter [ps]
250	3.9
400	4.1
500	4.75
800	6.98
1000	9.08

As for jitter dependency on noise frequency, Table IV and Fig.9 show the results obtained for a fixed H-field magnitude of  $173 dB\mu A/m$ . The behavior by increasing the frequency has been identified in a polynomial curve whose equation is reported in Fig.9.  $R^2$  in Fig.9 indicates the degree of accuracy of the proposed fitting method.

Moreover, experiments have been made to give a qualitative description of jitter's behavior for polarization issues between the forced H-field and the target board. While keeping the H-field generator (coil) at the same distance from the board, the angle between its magnetic axis and the board plane itself was varied. As shown in Fig.10, different angles are considered by pivoting the coil horizontally and vertically.

For example, Fig. 11 shows the jitter values obtained by applying a 250 KHz H-field with the magnitudes reported in Table III, and varying (Fig. 10) the angle "vertically" between the coil polar axis and the board. For different angles, the results show that the jitter is still linear with the H-field magnitude. However, different slopes correspond to different angles, thus highlighting different coupling effects. In particular, higher sensitivity is evident with an angle of 90 degrees between the coil axis and the board plane.

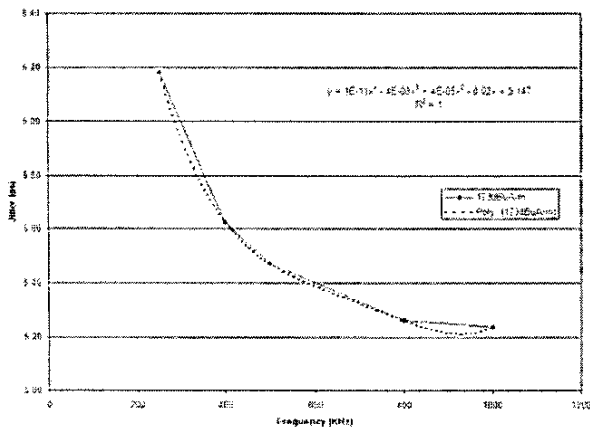


Fig. 9. Measured RMS jitter by applying a 173 dBu/m H-field at different frequency

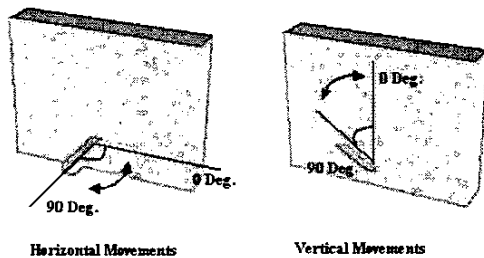


Fig. 10. Relative movements of the H-field generator with respect to the target board plane.

## V. CONCLUSION

As new generations of head boards are integrating most measurement functions (which in traditional ATEs were performed in the mainframe), higher accuracy can be achieved for high speed DUTs. However, the presence of nearby switching power supplies can potentially introduce jitter, and the jitter must be carefully controlled.

A jitter measurement methodology has been proposed; by analyzing the experimental results, it has been shown that a relationship exists for jitter variation with respect to EMI emission. To characterize the radiated electromagnetic noise in the head of an ATE, an external H-field generator has been designed. Experiments have been conducted by injecting onto the board H-fields of different magnitude and frequency. The corresponding jitter variations have been monitored.

Due to the operational features of an ATE the jitter was measured at the output of the head board using a daughter board, which was designed to circumvent ground noise and connectivity problems [1]. As per the Phase Noise model [7], the measurements have been made in a frequency domain, and converted to a time domain.

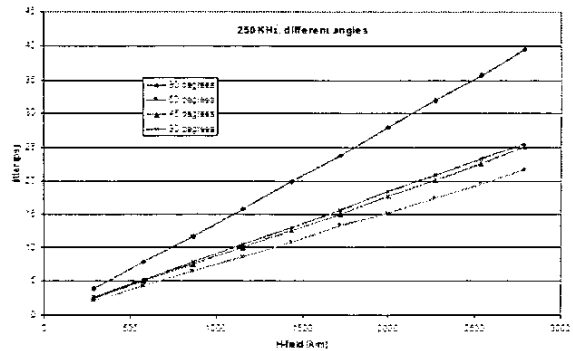


Fig. 11. Jitter measurements obtained by applying H-fields of increasing magnitude and fixed frequency (250 KHz) and varying the angle between the coil axis and the board plane with a vertical movement.

When the H-field strength is applied and varied at the loop filter of the PLL (which was previously identified as the most sensitive area of the head board), a jitter variation is observed. A direct relationship with the applied H-field has been established with the RMS jitter and the radiated EMI.

As for EMI interference it is anticipated that the framework provided by this research will be utilized to design ATE and head boards that can operate at very high frequencies.

## ACKNOWLEDGEMENT

This research has been supported by LTX Corporation of Westwood, Massachusetts, and by the International Test Conference Endowment at Northeastern University.

## REFERENCES

- [1] Y.J.Lee, T.Kane, J-J.Lim, L.Schiano, Y.-B.Kim, F.J.Meyer, F.Lombardi and S.Max "Analysis and Measurement of Timing Jitter Induced by Radiated EMI noise in ATE," in *IEEE Trans. on Inst. and Meas.*, vol.52, No.6, pp. 1749-1755, Dec.2003.
- [2] M. Goto and K. Hilliges, "The DFT age ATE architecture - The multiport ATE," in *Semicon. Semi Technical Symposium*, 2000.
- [3] M. Keating, "Fundamental Limits to Timing Accuracy," in *IEEE ITC Proceedings*, pp.756-762, 1986.
- [4] M. Mardiguian, *Controlling radiated emissions by design*, Kluwer Academic Publishers, 2nd edition, 2001
- [5] J. G. Kassakian, M. F. Schlecht, G. C. Verghese, *Principles of Power Electronics*, Addison Wesley, June 1992.
- [6] T. J. Yamaguchi et al, "A Method for Measuring the Cycle-to-Cycle Period Jitter of High -Frequency Clock Signals," in *19th IEEE VLSI Test Symposium Proceedings*, pp.174-177, 2001.
- [7] M. Shimanouchi, "An approach to Consistent Jitter Modeling for Various Jitter Aspects and Measurement Methods", in *IEEE ITC Proceedings*, pp.848-857, 2001.
- [8] R. Thottappillil, V. Seuka, J.Eriksson, A. Eriksson, and P. Ohman, "Estimation of fields radiated by a PCB from close magnetic field measurements", in *Int. Conf. on Electromagnetic Compatibility*, pp.89-93, 1997.
- [9] "Designing with LVDS", <http://www.national.com/appinfor/lvds>.
- [10] R. J. Baker, et al, "CMOS circuit design, layout, and simulation", *IEEE Press*, 1997.
- [11] B. P. Lathi, *Modern digital and analog communication systems*, Saunders College Publishing, 1989, 2nd edition.